Part of #4

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. ASMMC.036AUS	APPLICATION NO. 09/975,466
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	APPLICANT SOPHIE et al.	
(USE SEVERAL SHEETS IF NECESSARY)	FILING DATE October 9, 2001	GROUP 2812

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
EK	1	4,058,430	11/15/97	Suntola et al.	156	611	11/25/75
	2	5,711,811	01/27/98	Suntola et al.	118	711	11/28/95
	3	5,731,634	03/24/98	Matsuo et al.	257	752	06/06/96
	4	5,939,334	08/17/99	Nguyen et al.	438	689	05/22/97
	5	6,033,584	03/07/00	Ngo et al.	216	67	12/22/97
	6	6,066,892	05/23/00	Ding et al.	257	751	05/14/98
	7	6,124,189	09/26/00	Watanabe et al.	438	586	03/14/97
EK	8	6,130,123	10/10/00	Liang et al.	438	217	06/30/98

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
EK	9	0 469 470 A1	05.02.92	EP	—	—		
EK	10	EP 0 880 168 A2	25.11.98	EP	—	—		
EK	11	WO 93/10652	27.05.93	PCT	—	—		
EK	12	WO 00/03420	20.01.00	PCT	—	—		
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EK	19	Campbell, S.A. et al., "Titanium dioxide (TiO_2)-based gate insulators," IBM J. Res. Develop., Vol. 43, No. 3, pp. 383-392 (May 1999).
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EXAMINER Eric Cain	DATE CONSIDERED 10/10/02

*EXAMINER: INITIAL IF CITATION CONSIDERED, WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP 609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED, INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.

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EXAMINER INITIAL		OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
	22	Inoue, Noriaki, "Low thermal-budget fabrication of sputtered PZT capacitor on multilevel interconnects for embedded FeRAM," IEEE, IED 2000, Session 34 (2000).
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	24	Jung, D. et al., "A Novel Ir/IrO_2/Pt-PZT-Pt/IrO_2/Ir Capacitor for A Highly Reliable Mega-Scale FRAM," IEEE, IED 2000, Session 34, (2000).
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	28	Solanki R. et al., "Atomic Layer Deposition of Copper Seed Layers," Electrochemical and Solid-State Letters, Vol. 3, No. 10, pp. 479-480 (2000).
	29	Sundani et al., "Oral presentation of dual damascene process, slides.
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	34	Xu, P. et al., "A Breakthrough in Low-k Barrier/Etch Stop Films for Copper Damascene Applications," Semiconductor Fabtech, 11th Edition, p. 239 (2000).
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	36	Yoon, Dong-Soo et al., "Investigation of RuO_2-Incorporated Pt Layer as a Bottom Electrode and Diffusion Barrier for High Epsilon Capacitor Applications," Electrochemical and Solid-State Letters, Vol. 3, No. 8, pp. 373-376 (2000).
EK	37	Yoon, Y.-G. et al., 197th Meeting Program Information II, The Electrochemical Society, 197th Meeting – Toronto, Ontario, Canada, May 14-18, 2000, Program Information, I1 – Rapid Thermal and Other Short-Time Processing Technologies I, Electronics Division/Dielectric Science and Technology Division/High Temperature Materials Division, 2000, Wednesday, May 17, 2000, New Applications of RTP, Co-Chairs: A. Fiory and D.-L. Kwong, Time 11:10 Abs#550, Title: Development of RTA Process for the Crystallization of a-Si Thin Film – Y.-G. Yoon, T.-K. Kim, K.-B. Kim, C.-Y. Cho, B.-I. Lee, and S.-K. Joo (Seoul National Univ.)

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EXAMINER Eric Kielin	DATE CONSIDERED 10/10/02

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
EK	1.	US 2001/0018266 A1	08/30/01	Jiang et al.	438	678	05/09/01
	2.	6,303,500 B1	10/16/01	Jiang et al.	438	678	02/24/99
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	4.	US 2001/0052318 A1	12/20/01	Jiang et al.	118	403	08/01/01
EK	5.	US 6,346,151 B1	02/12/02	Jiang et al.	118	403	12/16/99

FOREIGN PATENT DOCUMENTS

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EXAMINER INITIAL		**OTHER DOCUMENTS** (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

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EXAMINER Eric Kielin	DATE CONSIDERED 10/10/02

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